MCS9901 PCI Express to Peripheral Controller

Data Sheet

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MCS9901

PCIe to Peripheral Controller

1. Features

PCI Express

- Fully compliant with PCI Express Base Specification, Revision 1.0a
- Compatible for PCI Express Card application requirements
- PCIe Multi Function Peripheral Controller with x1 Lane Interface
- Supports four PCIe functions
- Support for D1, D2, D3hot and D3cold
- Utilizes 100-MHz Differential PCI Express Common Reference Clock
- Supports PCIe Power Management

Serial Port

- Four 16C 450/550/Extended 550 compatible UARTs
- Supports RS232, RS485 & RS422 modes
- Bi-directional speeds from 50 bps to 16 Mbps/Port
- Full Serial modem control
- Supports Hardware, Software flow control
- 5, 6, 7, 8 and 9-bit Serial format support
- Even, Odd, None, space & Mark parity supported
- Custom BAUD Rates supported with external clock or by programming internal PLL
- On Chip 256 Byte depth FIFOs in Transmit, Receive path of each Serial Port
- Supports power management features
- Serial Port transceiver shutdown support
- Supports Slow IrDA on all Serial Ports

IEEE1284 Parallel Port

- Multi-mode IEEE1284 compliant controller (SPP, PS2, EPP, ECP)
- Faster data rates up to 1.5Mbps for parallel port

ISA

- ISA style I/O interface for extending UARTs & Parallel Ports
- 8-bit data bus @ 8Mhz

USB

- One high-speed USB Host Controller (USB 2.0)
- Supports OHCI & EHCI Interfaces
- Can be interfaced with external ULPI High Speed USB PHY for USB Port expansion

Miscellaneous

- Two-Wire I^2C Interface for EEPROM
- EEPROM read/write through PCIe interface
- Eight bi-directional multi-function GPIO lines
- On chip oscillator

2. Applications

- Serial Attached Devices
- Serial Networking/Monitoring Equipment
- Data Acquisition System
- POS Terminal & Industrial PC
- Parallel/Printer Port based applications
- Add-On I/O Cards – Serial/Parallel/ USB
- Embedded systems – For I/O expansion

3. Ordering Information

- Part Number : MCS9901CV-AA
- 128 Pin QFP
- ROHS
- Commercial Grade, 0 to 70 deg C

4. Application Schematic

- PCIe to 4 Serial
- PCIe to 2S + 1 Parallel
- PCIe to 2S + 4 Serial by ISA
- PCIe to USB + 2S

5. Evaluation Board

- MCS9901 - EVB - 4S
- MCS9901 - EVB - 2S + 1P
- MCS9901 - EVB - 6S
- MCS9901 - EVB - USB + 2S

6. Software Support

SW Driver Support

- Windows 32bit 2000/XP/2003 Server
- Windows 64bit XP/2003 Server
- Windows Vista 32 & 64bit
- Linux Kernel 2.6.11 & above
- MAC 10.4.X & above

SW Utility Support

- Windows-XP based EEPROM Utility
- Windows-XP based Diagnostic Utility

7. Certifications

- WHQL Certification for Windows XP/ Vista device drivers
- PCI Express compliance – MCS9901 certified for PCIe compliance through MosChip MCS9901-EVB-4S.

8. General Description

MCS9901 is a single lane PCI Express (PCIe) to Peripheral Controller. It is a single chip solution for PCIe-based Serial/Parallel port expansion add-in cards. MCS9901 supports four high performance serial ports namely; one IEEE 1284 compliant Parallel Port, one USB 2.0 host controller and ISA style interface. It is ideally suited for desktop PCs and notebook applications such as add-in Cards/ Express Cards for high-speed Serial/Parallel/ USB port expansion.

The PCI Express interface of MCS9901 is fully compliant with PCI Express base 1.0a specifications. It supports four functions with a single device.

Each serial port of MCS9901 supports extended 16C550 UART mode and supports serial speeds up to 16Mbps. An individual serial port has a FIFO depth of 256 bytes each for transmit and receive paths.

Deeper FIFOs enable high serial speeds/ throughputs and reduce CPU utilization. Each serial port is compatible with industry standard 16C550 devices including MosChip family of UARTs such as MCS9835, MCS9845, MCS9820, MCS7840, MCS7820, MCS7720 and MCS7703.

The Parallel Port interface is IEEE 1284 compliant and supports SPP/PS2/EPP/ECP modes and Centronics interface.

Integrated High speed USB Host Controller (USB 2.0) interface can be used with an external ULPI USB PHY for providing USB port over PCIe interface.

ISA Style interface is designed to add additional Serial/Parallel ports by using external ISA peripherals. ISA interface can be used to follow the Serial/Parallel port expansion through ISA: 1 to 4 Serial or 1 Serial + 1 Parallel or 2 Serial + 1 Parallel.

MCS9901 has 4 mode select pins. These can be bonded at the system level to configure MCS9901 for the following configurations:

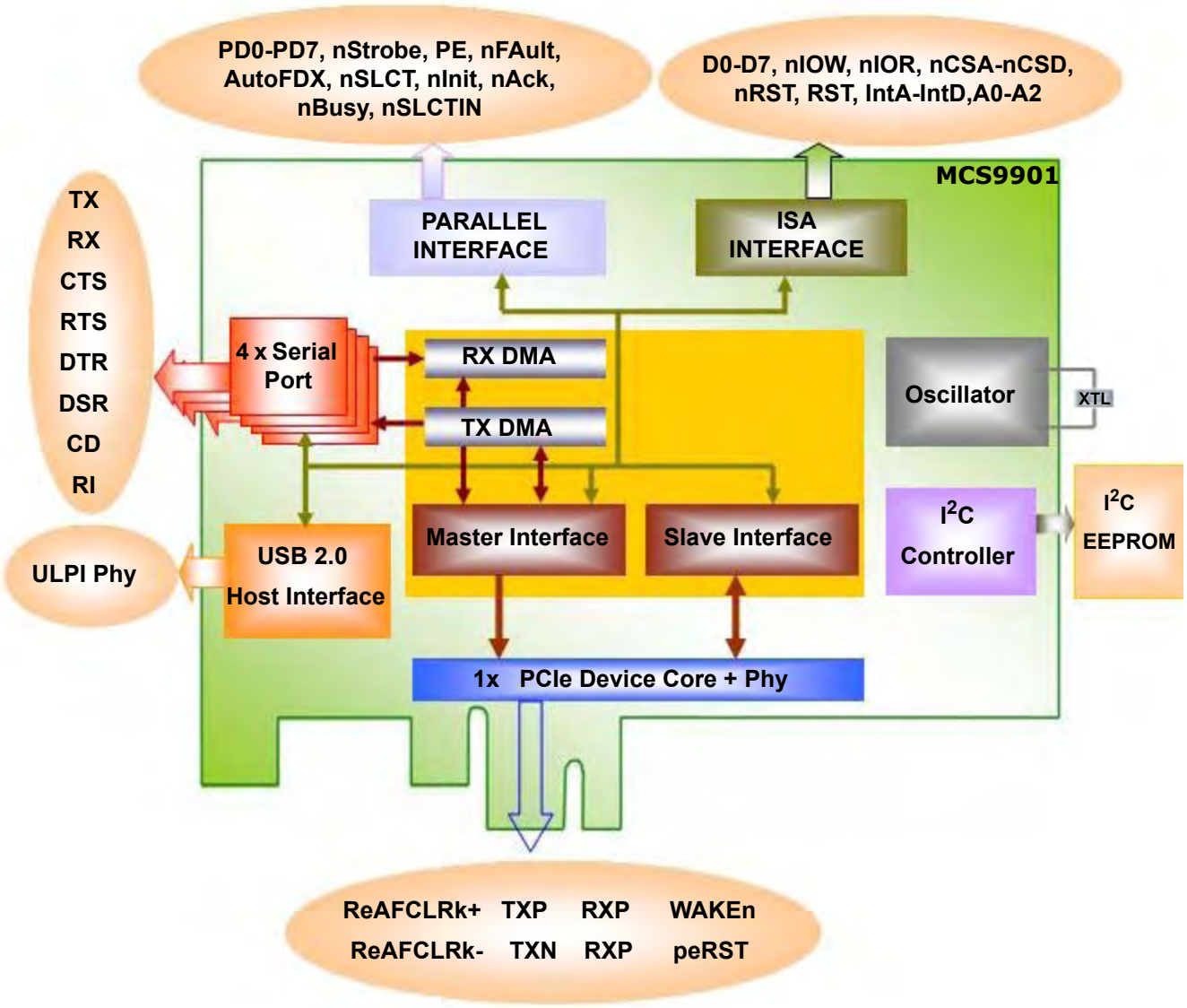
- PCIe to 4 Serial
- PCIe to 2 Serial + 1 Parallel
- PCIe to 2 Serial + ISA
- PCIe to USB + 2S
- PCIe to USB + 1P
- PCIe to USB + ISA
- PCIe to USB

All the configurations listed above can be achieved through system level mode selection by 4 mode select pins.

When ISA mode is selected, MCS9901 assumes the presence of an external "ISA to 4 Serial" peripheral on the ISA interface as default configuration and this combination can be supported without an external EEPROM. External EEPROM is needed for other ISA based Serial/Parallel combinations.

Many other Serial/Parallel port configurations can be supported by using external EEPROM. Refer to **Section 17** for details.

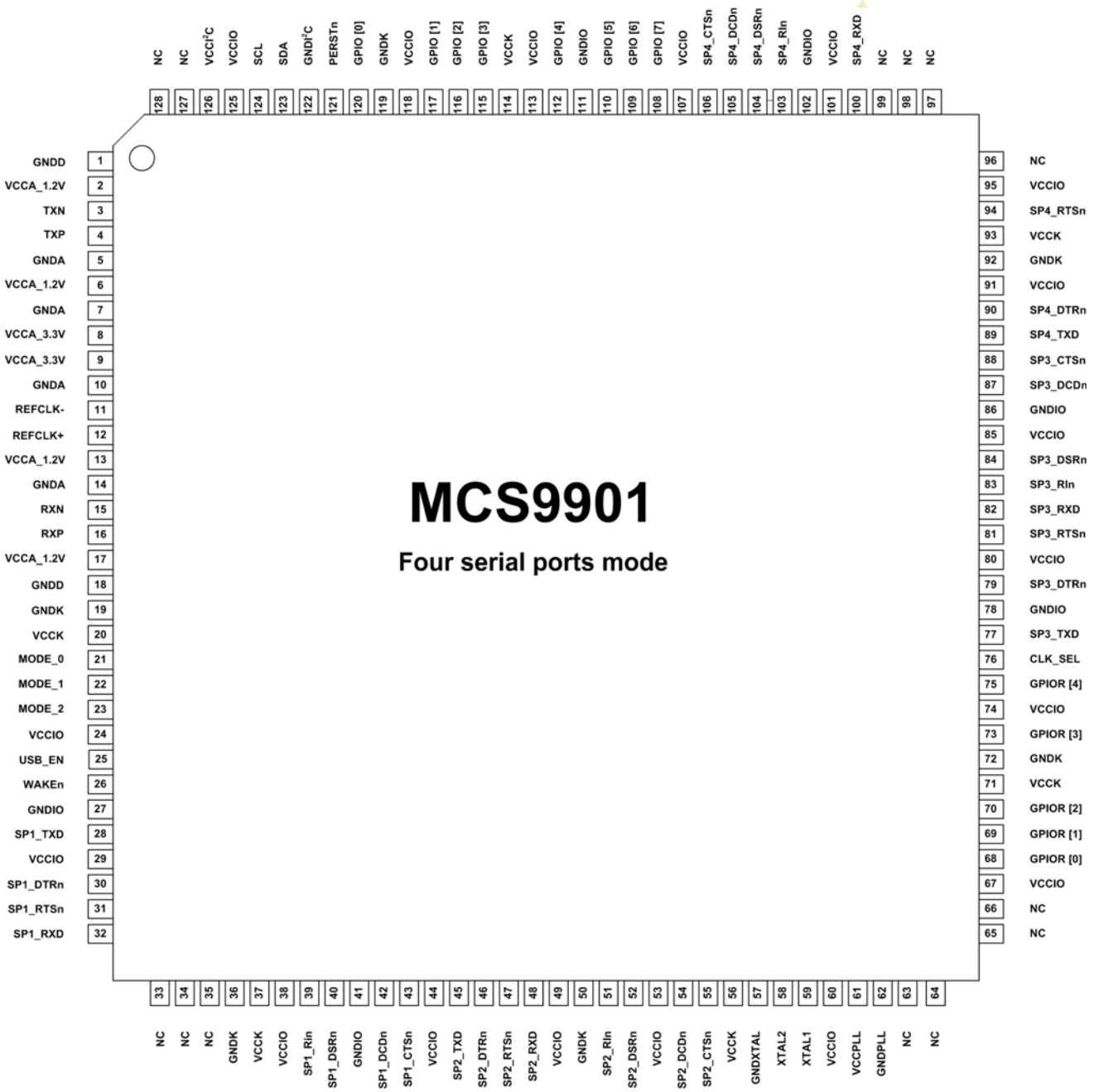
9. Block Diagram



10. Pin Out Diagrams

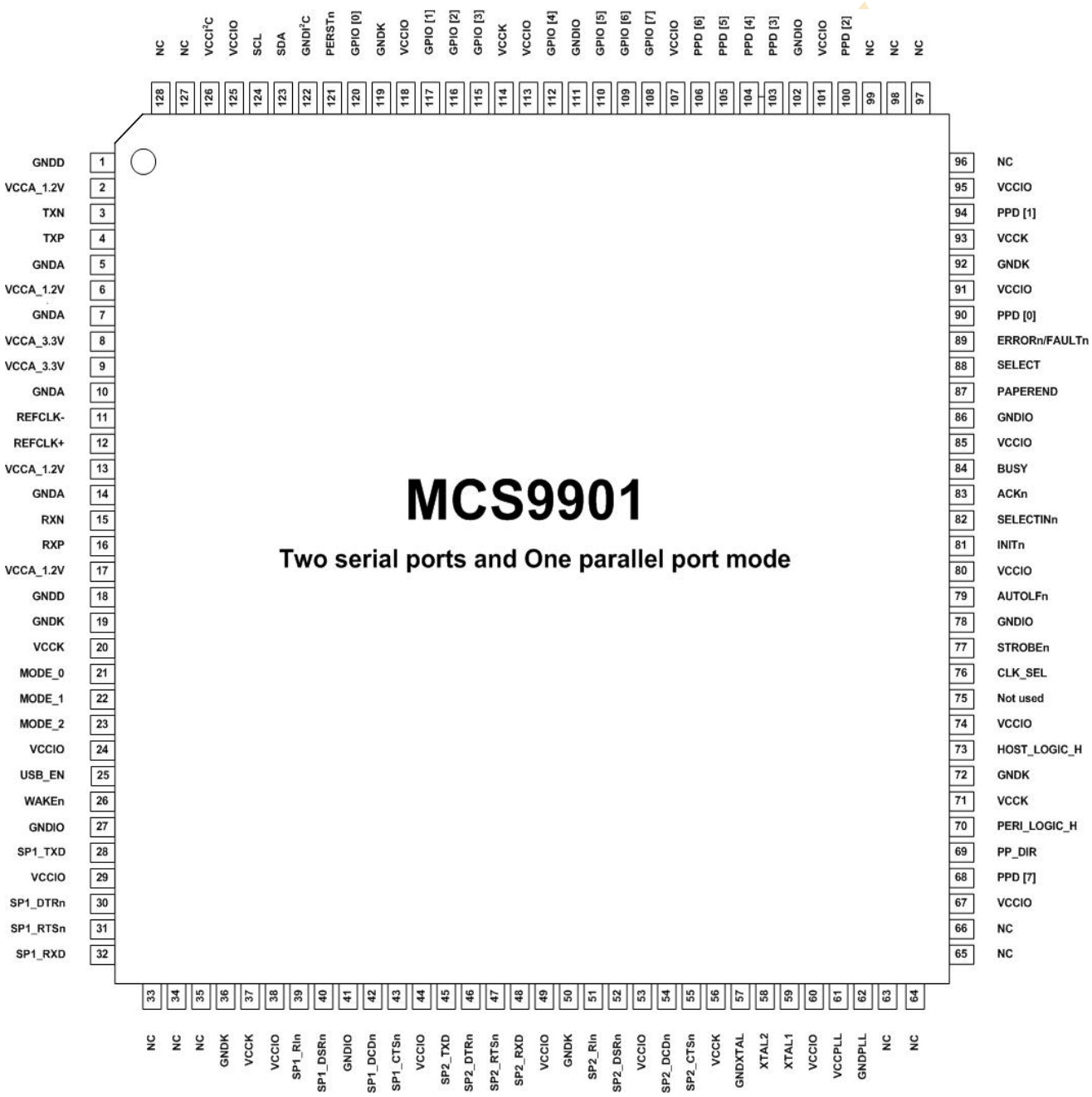
10.1 Four serial ports mode

(USB_EN = GNDIO, MODE_2 = GNDIO, MODE_1 = GNDIO, MODE_0= VCCIO)



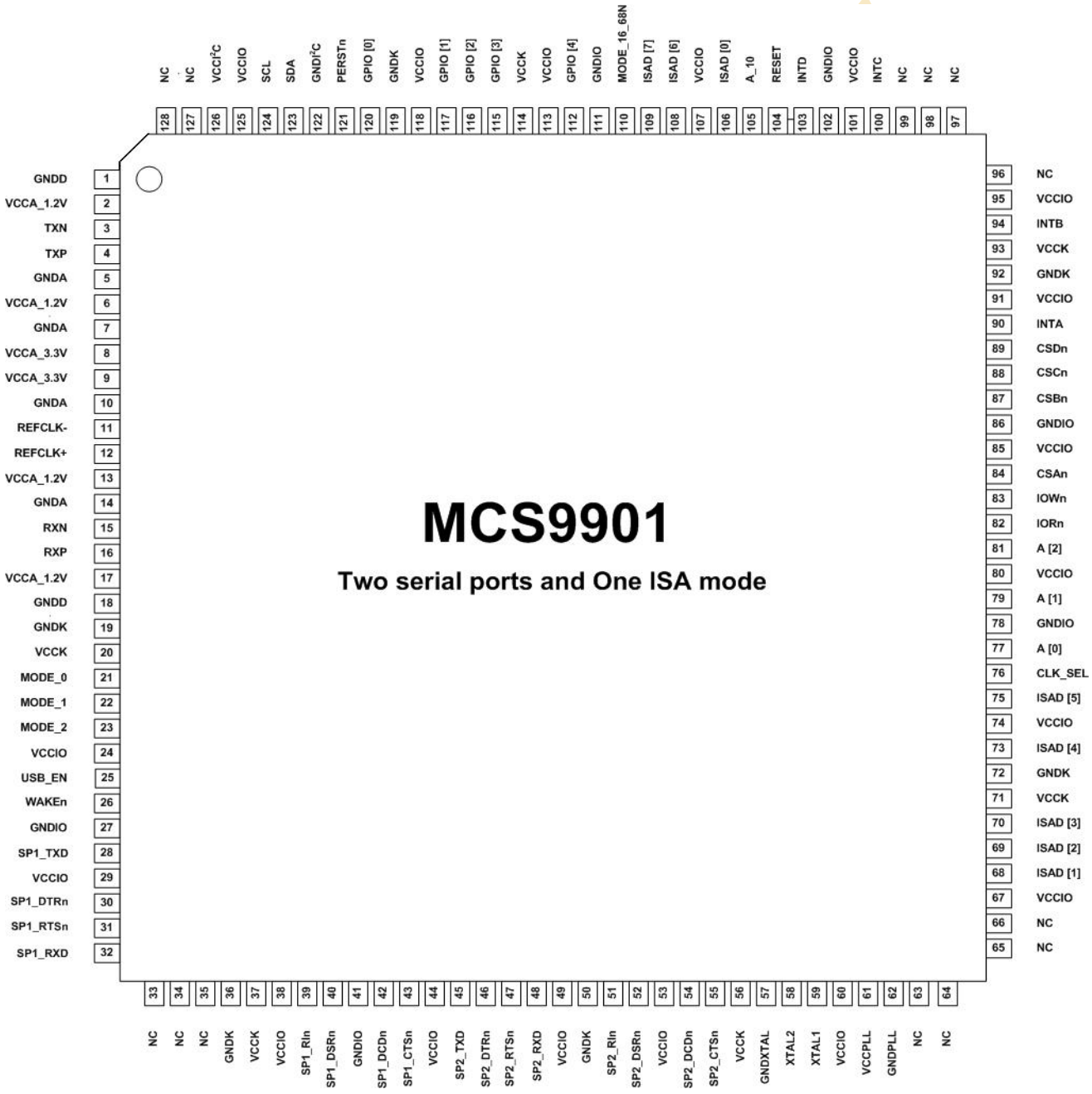
10.2 Two serial ports and One parallel port mode

(USB_EN = GNDIO, MODE_2 = GNDIO, MODE_1 = VCCIO, MODE_0= GNDIO)



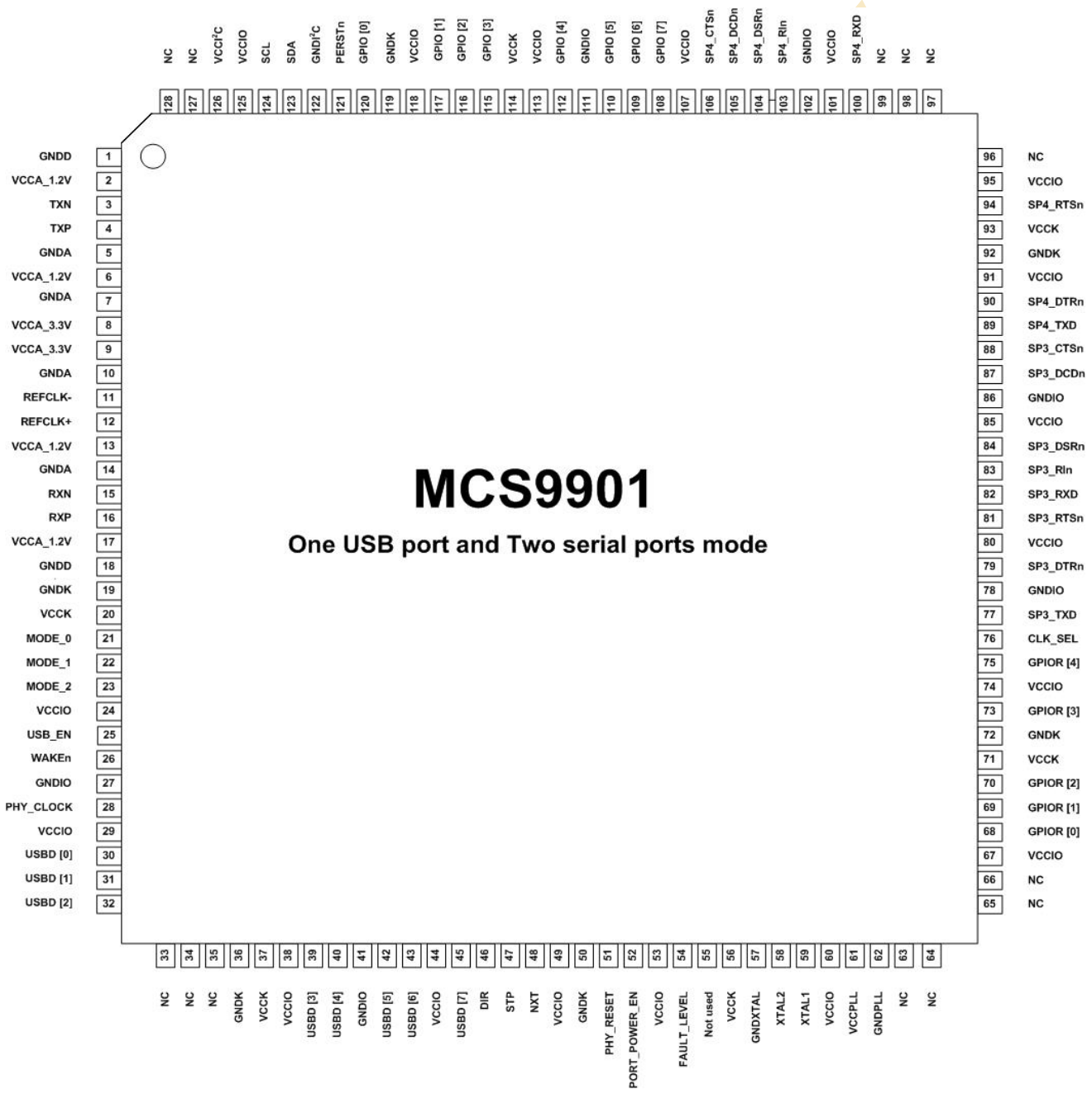
10.3 Two serial ports and One ISA mode

(USB_EN = GNDIO, MODE_2 = GNDIO, MODE_1 = VCCIO, MODE_0= VCCIO)



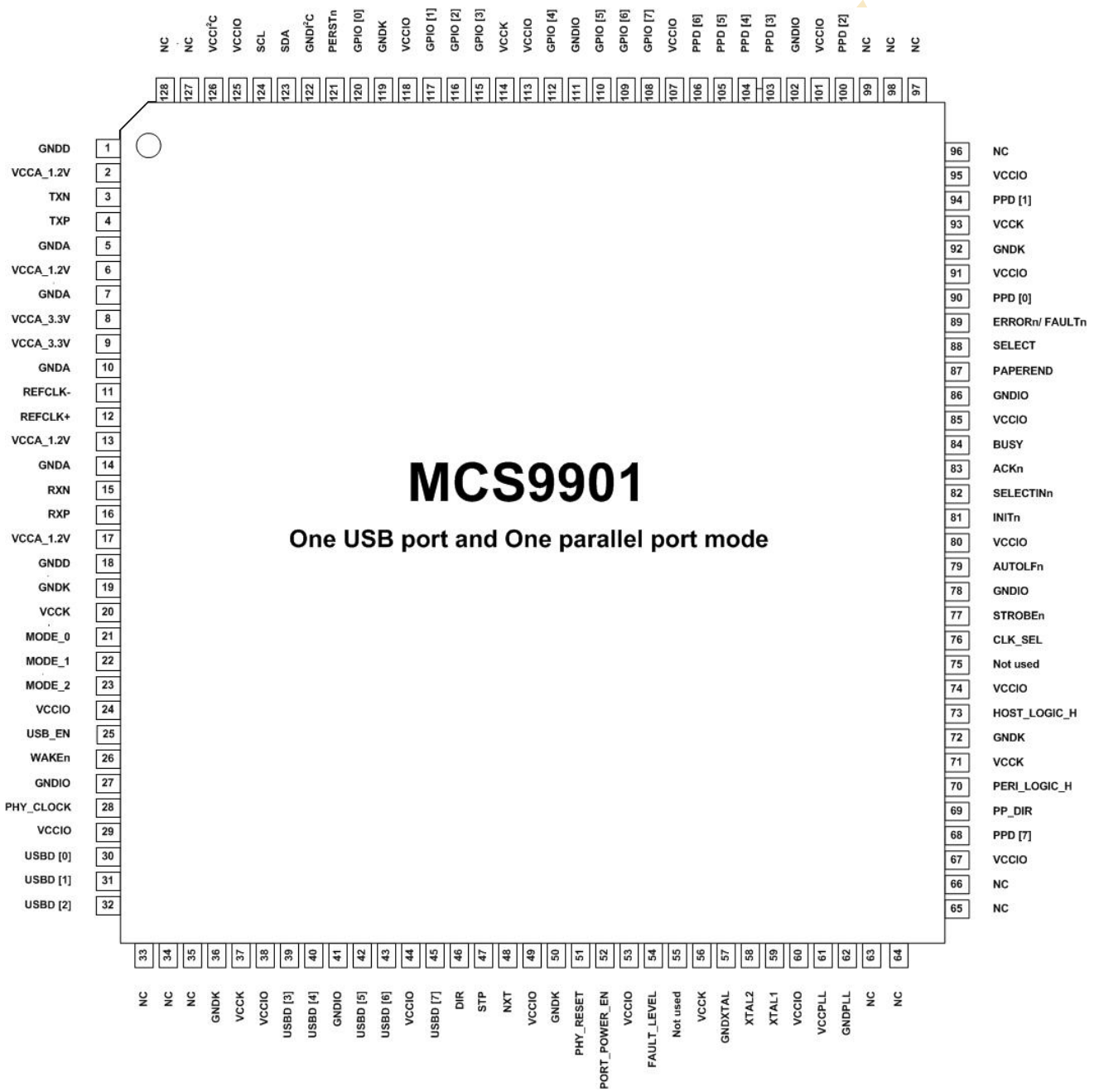
10.4 One USB port and Two serial ports mode

(USB_EN = VCCIO, MODE_2 = GNDIO, MODE_1 = GNDIO, MODE_0= VCCIO)



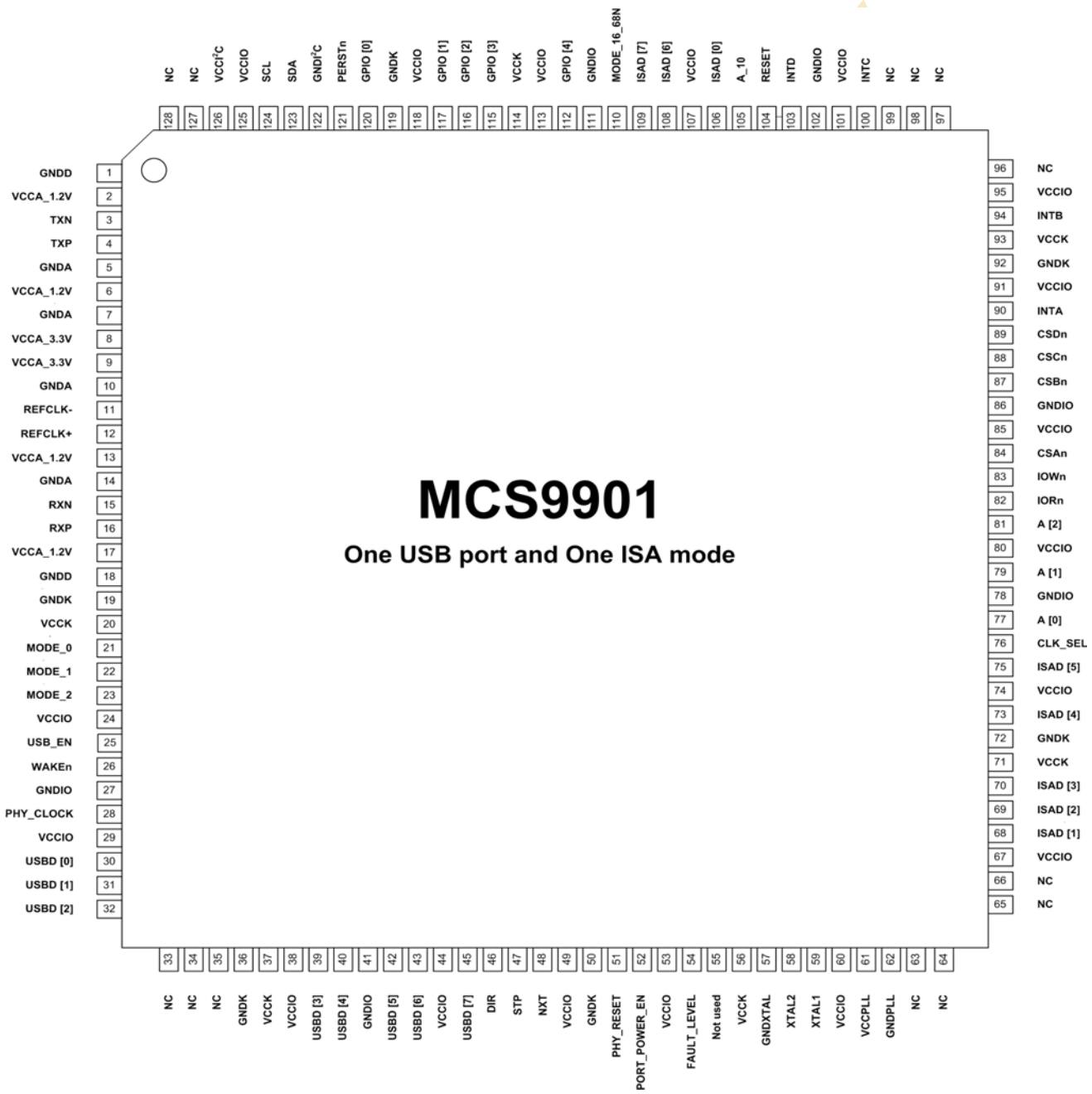
10.5 One USB port and One parallel port mode

(USB_EN = VCCIO, MODE_2 = GNDIO, MODE_1 = VCCIO, MODE_0= GNDIO)



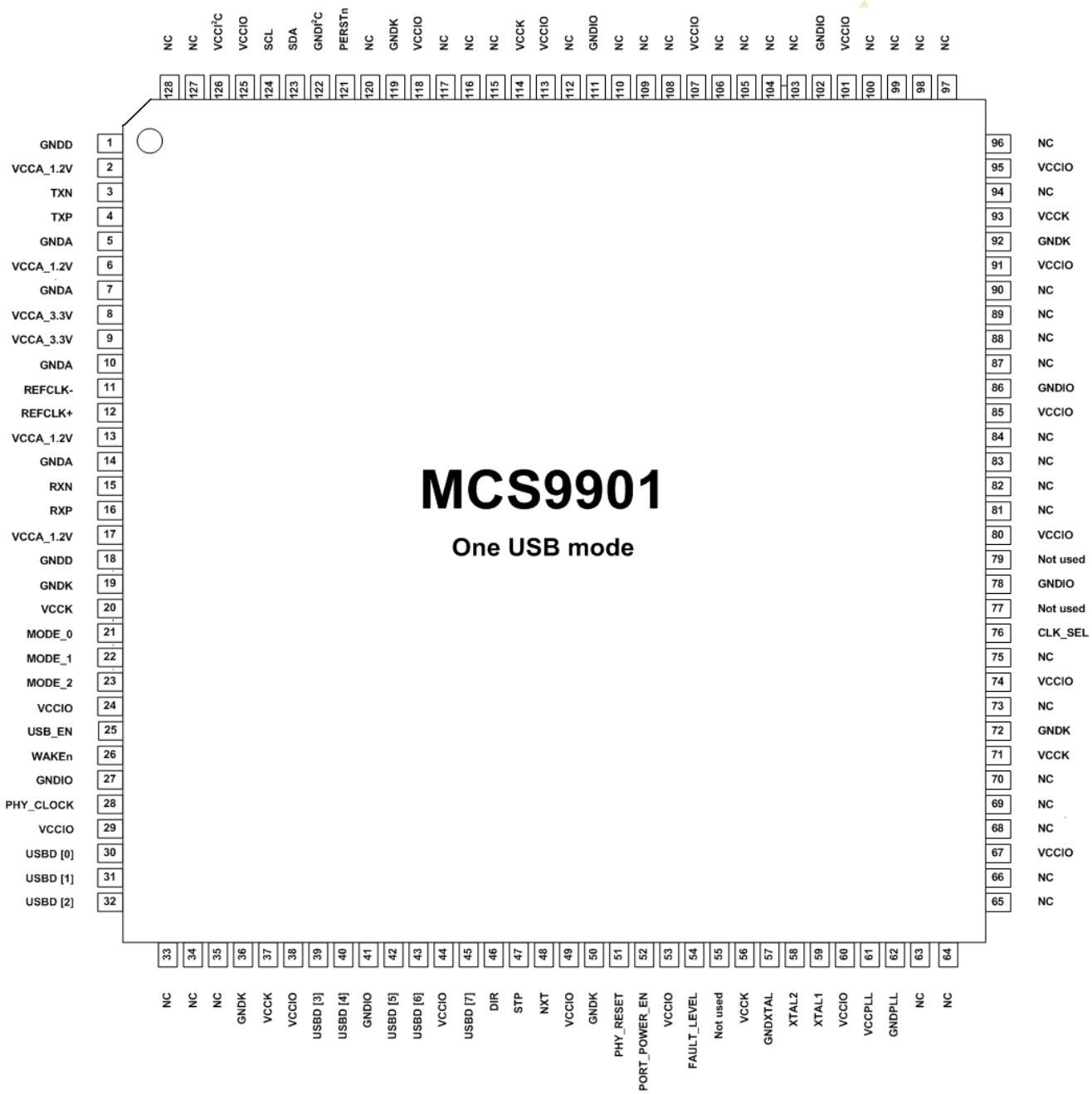
10.6 One USB port and One ISA mode

(USB_EN = VCCIO, MODE_2 = GNDIO, MODE_1 = VCCIO, MODE_0= VCCIO)



10.7 One USB mode

(USB_EN = VCCIO, MODE_2 = VCCIO, MODE_1 = VCCIO, MODE_0= GNDIO)



11. Pin Descriptions

This section provides information on each pin of MCS9901 (QFP 128). To facilitate detailing, pin descriptions have been classified into 5 different groups:

- PCI Express Signals
- Multiplexed Interface Signals
- Mode Select, Clock, Reset and Miscellaneous Signals
- Power and Ground Signals
- No Connect Signals

11.1 PCI Express Signals

Table 1: PCI Express Signals

Pin Number	Pin Name	Type	Description
26	WAKEn	O	To be Left unconnected at system level.
16	RXP	I	PCIe PHY differential positive serial data input.
15	RXN	I	PCIe PHY differential negative serial data input.
12	REFCLK+	I	PCIe PHY differential PLL reference clock.
11	REFCLK-	I	PCIe PHY differential PLL reference clock.
4	TXP	O	PCIe PHY differential positive serial data output.
3	TXN	O	PCIe PHY differential negative serial data output.
76	CLK_SEL	O	Used to enable/disable clock of PCI Express card.

11.2 Multiplexed Interface Signals

Table 2 lists the Multiplexed Interface Signal description for the concerned pin numbers. The functionality of multiplexed signal depends on the settings of mode select pins. The operation of MCS9901 is broadly classified into 7 different modes. This classification is detailed in Table 2, below.

Specific details of mode select pins can be seen in Table 6. Detailed description for the different signals is listed in Table 7 (E.g.: Detailed description of signal “SP1_TXD”).

Table 2: Multiplexed Interface Signals

Pin Number	Multiplexed Interface Signal Descriptions as per Selected Mode						
	4SP	2SP-1PP	2SP-ISA	USB-2SP	USB-1PP	USB-ISA	USB-ONLY
28	SP1_TXD	SP1_TXD	SP1_TXD	PHY_ CLOCK	PHY_ CLOCK	PHY_ CLOCK	PHY_ CLOCK
30	SP1_DTRn	SP1_DTRn	SP1_DTRn	USBD [0]	USBD [0]	USBD [0]	USBD [0]
31	SP1_RTSn	SP1_RTSn	SP1_RTSn	USBD [1]	USBD [1]	USBD [1]	USBD [1]
32	SP1_RXD	SP1_RXD	SP1_RXD	USBD [2]	USBD [2]	USBD [2]	USBD [2]
39	SP1_RIn	SP1_RIn	SP1_RIn	USBD [3]	USBD [3]	USBD [3]	USBD [3]
40	SP1_DSRn	SP1_DSRn	SP1_DSRn	USBD [4]	USBD [4]	USBD [4]	USBD [4]
42	SP1_DCDn	SP1_DCDn	SP1_DCDn	USBD [5]	USBD [5]	USBD [5]	USBD [5]
43	SP1_CTSn	SP1_CTSn	SP1_CTSn	USBD [6]	USBD [6]	USBD [6]	USBD [6]
45	SP2_TXD	SP2_TXD	SP2_TXD	USBD [7]	USBD [7]	USBD [7]	USBD [7]
46	SP2_DTRn	SP2_DTRn	SP2_DTRn	DIR	DIR	DIR	DIR
47	SP2_RTSn	SP2_RTSn	SP2_RTSn	STP	STP	STP	STP
48	SP2_RXD	SP2_RXD	SP2_RXD	NXT	NXT	NXT	NXT
51	SP2_RIn	SP2_RIn	SP2_RIn	PHY_ RESET	PHY_ RESET	PHY_ RESET	PHY_ RESET
52	SP2_DSRn	SP2_DSRn	SP2_DSRn	Port _ Power_EN	Port_ Power_EN	Port_ Power_EN	Port_ Power_EN
54	SP2_DCDn	SP2_DCDn	SP2_DCDn	Fault_ Level	Fault_ Level	Fault_ Level	Fault_ Level
55	SP2_CTSn	SP2_CTSn	SP2_CTSn	Not used	Not used	Not used	Not used
77	SP3_TXD	STROBEn	A [0]	SP3_TXD	STROBEn	A [0]	Not used
79	SP3_DTRn	AUTOLFn	A [1]	SP3_DTRn	AUTOLFn	A [1]	Not used
81	SP3_RTSn	INITn	A [2]	SP3_RTSn	INITn	A [2]	NC
82	SP3_RXD	SELECTINn	IORn	SP3_RXD	SELEC-TINn	IORn	NC

Table 2: Multiplexed Interface Signals (Contd.)

Pin Number	Multiplexed Interface Signal Descriptions as per Selected Mode						
	4SP	2SP-1PP	2SP-ISA	USB-2SP	USB-1PP	USB-ISA	USB-ONLY
83	SP3_RIn	ACKn	IOWn	SP3_RIn	ACKn	IOWn	NC
84	SP3_DSRn	BUSY	CSAn	SP3_DSRn	BUSY	CSAn	NC
87	SP3_DCDn	PAPEREND	CSBn	SP3_DCDn	PAPEREND	CSBn	NC
88	SP3_CTSn	SELECT	CSCn	SP3_CTSn	SELECT	CSCn	NC
89	SP4_TXD	ERRORn/ FAULTn	CSDn	SP4_TXD	ERRORn/ FAULTn	CSDn	NC
90	SP4_DTRn	PPD [0]	INTA	SP4_DTRn	PPD [0]	INTA	NC
94	SP4_RTSn	PPD [1]	INTB	SP4_RTSn	PPD [1]	INTB	NC
100	SP4_RXD	PPD [2]	INTC	SP4_RXD	PPD [2]	INTC	NC
103	SP4_RIn	PPD [3]	INTD	SP4_RIn	PPD [3]	INTD	NC
104	SP4_DSRn	PPD [4]	RESET	SP4_DSRn	PPD [4]	RESET	NC
105	SP4_DCDn	PPD [5]	A_10	SP4_DCDn	PPD [5]	A_10	NC
106	SP4_CTSn	PPD [6]	ISAD [0]	SP4_CTSn	PPD [6]	ISAD [0]	NC
68	GPIOR [0]	PPD [7]	ISAD [1]	GPIOR [0]	PPD [7]	ISAD [1]	NC
69	GPIOR [1]	PP_DIR	ISAD [2]	GPIOR [1]	PP_DIR	ISAD [2]	NC
70	GPIOR [2]	PERI_ LOGIC_H	ISAD [3]	GPIOR [2]	PERI_ LOGIC_H	ISAD [3]	NC
73	GPIOR [3]	HOST_ LOGIC_H	ISAD [4]	GPIOR [3]	HOST_ LOGIC_H	ISAD [4]	NC
75	GPIOR [4]	Not used	ISAD [5]	GPIOR [4]	Not used	ISAD [5]	NC
108	GPIO [7]	GPIO [7]	ISAD [6]	GPIO [7]	GPIO [7]	ISAD [6]	NC
109	GPIO [6]	GPIO [6]	ISAD [7]	GPIO [6]	GPIO [6]	ISAD [7]	NC
110	GPIO [5]	GPIO [5]	MODE_ 16_68N	GPIO [5]	GPIO [5]	MODE_ 16_68N	NC
112	GPIO [4]	GPIO [4]	GPIO [4]	GPIO [4]	GPIO [4]	GPIO [4]	NC
115	GPIO [3]	GPIO [3]	GPIO [3]	GPIO [3]	GPIO [3]	GPIO [3]	NC
116	GPIO [2]	GPIO [2]	GPIO [2]	GPIO [2]	GPIO [2]	GPIO [2]	NC

Table 2: Multiplexed Interface Signals (Contd.)

Pin Number	Multiplexed Interface Signal Descriptions as per Selected Mode						
	4SP	**2SP-1PP**	**2SP-ISA**	**USB-2SP**	**USB-1PP**	**USB-ISA**	**USB-ONLY**
117	GPIO [1]	GPIO [1]	GPIO [1]	GPIO [1]	GPIO [1]	GPIO [1]	NC
120	GPIO [0]	GPIO [0]	GPIO [0]	GPIO [0]	GPIO [0]	GPIO [0]	NC

Note: SP - Serial Port; PP - Parallel Port; ISA - Industry Standard Architecture; USB - Universal Serial Bus.

11.3 Mode Select, Clock, Reset, and Miscellaneous Signals

Table 3: Mode Select, Clock, Reset and Miscellaneous Signals

Pin Number	Pin Name	Type	Description
25	USB_EN	I	USB selection input. It should be hard-wired to either GNDIO or VCCIO as per functional mode requirements. Refer to **Table 6** for details
23	MODE_2	I	Mode Selection input (2). It should be hard-wired to either GNDIO or VCCIO as per functional mode requirements. Refer to **Table 6** for details
22	MODE_1	I	Mode Selection input (1). GNDIO or VCCIO as per functional mode requirements. Refer to **Table 6** for details
21	MODE_0	I	Mode Selection input (0). GNDIO or VCCIO as per functional mode requirements. Refer to **Table 6** for details
59	XTAL1	I	Crystal oscillator input or external clock input. This input signal is used in conjunction with XTAL2 to form a feedback circuit for the internal timing. Two external capacitors connected from each side of the XTAL1 and XTAL2 to GND are required to form a crystal oscillator circuit
58	XTAL2	I/O	Crystal oscillator output. See XTAL1 description
121	PERSTn	I	Power on reset signal, Active low signal
124	SCL	I/O	2-Wire EEPROM Clock, needs 4K7 pull-up resistor to 3.3V
123	SDA	I/O	2-Wire EEPROM Data in/out, needs 4K7 pull-up resistor to 3.3V

11.4 Power and Ground Signals

Table 4: Power and Ground Signals

Pin Number	Pin Name	Type	Description
20,114,93,71,56, 37	VCCK	Power	1.2V Core supply
19,119,92,72,50, 36	GNDK	Ground	Core ground
126	VCCI^{2}C	Power	1.2V I^{2}C I/O supply
122	GNDI^{2}C	Ground	I^{2}C I/O Ground
29,24,125,118, 113,107,101,95, 91,85,80,74,67, 60,53,49,44,38	VCCIO	Power	3.3V I/O Supply
27,111,102,86, 78,41	GNDIO	Ground	I/O ground
62	GNDPLL	Ground	PLL ground.
61	VCCPLL	Power	1.2V PLL supply.
17,13,6,2	VCCA_1.2V	Power	1.2V, Analog voltage supply
9,8	VCCA_3.3V	Power	3.3V, Analog voltage supply
18,1	GNDD	Ground	Digital GND
14,10,7,5	GNDA	Ground	Analog voltage GND
57	GNDXTAL	Ground	Crystal oscillator ground

11.5 No Connect Pins

Table 5: No Connect Pins

Pin Number	Type	Description
33,34,35,63,64,65, 66,96,97,98,99, 127,128	Reserved	These are no connect pins & to be left as No Connects in system design. Do not connect any of these pins to any other signal / pin / Ground / Supply.

12. Mode Selection – System Level Settings

Table 6: Mode Selection – System Level Settings

Configuration	USB_EN	MODE_2	MODE_1	MODE_0	Remarks
4SP	0	0	0	1	PID = 9901
2SP-1PP	0	0	1	0	PID = 9901
2SP-ISA	0	0	1	1	PID = 9901
USB-2SP	1	0	0	1	PID = 9902
USB-1PP	1	0	1	0	PID = 9902
USB-ISA	1	0	1	1	PID = 9902
USB-ONLY	1	1	1	0	PID = 9920

In the above table, "0" refers to a particular pin being connected to "GNDIO" and "1" refers to a particular pin being connected to "VCCIO".

PID – Product ID. MCS9901 PCIe to Peripheral controller reports different PID values to the PCIe Bus as per mode selection pins settings. Refer to remarks column in Table 6.

13. Description of Multiplexed Signals

Table 7: Multiplexed Signals Description

Signal Name	Group	Type	Drive Strength	Description
SP1_ CTSn	SP	I	4 mA	Serial Port 1 Clear To Send (in serial protocol), active low
SP1_ DCDn	SP	I	4 mA	Serial Port 1 Data Carrier Detect (in serial protocol), active low
SP1_ DSRn	SP	I	4 mA	Serial Port 1 Data Set Ready (in serial protocol), active low
SP1_DTRn	SP	O	4 mA	Serial Port 1 Data Terminal Ready (in serial protocol), active low
SP1_RIn	SP	I	4 mA	Serial Port 1 Ring Indicator, active low
SP1_RTSn	SP	O	4 mA	Serial Port 1 Request To Send (in serial protocol), active low

Table 7: Multiplexed Signals Description (Contd.)

Signal Name	Group	Type	Drive Strength	Description
SP1_RXD	SP	I	4 mA	Serial Port 1 Serial Receive Data from transceiver or IrDA data in from IrDA detector
SP1_TXD	SP	O	4 mA	Serial Port 1 Transmit Data to transceiver, or IrDA data out to IR LED
SP2_ CTSn	SP	I	4 mA	Serial Port 2 Clear To Send (in serial protocol), active low
SP2_ DCDn	SO	I	4 mA	Serial Port 2 Data Carrier Detect (in serial protocol), active low
SP2_ DSRn	SP	I	4 mA	Serial Port 2 Data Set Ready (in serial protocol), active low
SP2_ DTRn	SP	O	4 mA	Serial Port 2 Data Terminal Ready (in serial protocol), active low
SP2_ RTSn	SP	O	4 mA	Serial Port 2 Request To Send (in serial protocol), active low
SP2_ RXD	SP	I	4 mA	Serial Port 2 Serial Receive Data from transceiver or IrDA data in from IrDA detector
SP2_ TXD	SP	O	4 mA	Serial Port 2 Transmit Data to transceiver, or IrDA data out to IR LED
SP2_RIn	SP	I	4 mA	Serial Port 2 Ring Indicator, active low
SP3_ CTSn	SP	I	4 mA	Serial Port 3 Clear To Send (in serial protocol), active low
SP3_ DCDn	SP	I	4 mA	Serial Port 3 Data Carrier Detect (in serial protocol), active low
SP3_ DSRn	SP	I	4 mA	Serial Port 3 Data Set Ready (in serial protocol), active low
SP3_ DTRn	SP	O	11 mA	Serial Port 3 Data Terminal Ready (in serial protocol), active low
SP3_ RTSn	SP	O	11 mA	Serial Port 3 Request To Send (in serial protocol), active low
SP3_ RXD	SP	I	11 mA	Serial Port 3 Serial Receive Data from transceiver or IrDA data in from IrDA detector

Table 7: Multiplexed Signals Description (Contd.)

Signal Name	Group	Type	Drive Strength	Description
SP3_ TXD	SP	O	11 mA	Serial Port 3 Transmit Data to transceiver, or IrDA data out to IR LED
SP3_RIn	SP	I	4 mA	Serial Port 3 Ring Indicator, active low
SP4_ DTRn	SP	O	11 mA	Serial Port 4 Data Terminal Ready (in serial protocol), active low
SP4_ RTSn	SP	O	11 mA	Serial Port 4 Request To Send (in serial protocol), active low
SP4_ RXD	SP	I	11 mA	Serial Port 4 Serial Receive Data from transceiver or IrDA data in from IrDA detector
SP4_ TXD	SP	O	4 mA	Serial Port 4 Transmit Data to transceiver, or IrDA data out to IR LED
SP4_CTSn	SP	I	11 mA	Serial Port 4 Clear To Send (in serial protocol), active low
SP4_DCDn	SP	I	11 mA	Serial Port 4 Data Carrier Detect (in serial protocol), active low
SP4_DSRn	SP	I	11 mA	Serial Port 4 Data Set Ready (in serial protocol), active low
SP4_RIn	SP	I	11 mA	Serial Port 4 Ring Indicator, active low
GPIOR [0]	-	I/O	11 mA	This pin can be used as GPIO when Parallel, ISA modes are not used.
GPIOR [4:1]	-	I/O	4 mA	These pins can be used as GPIO when Parallel, ISA modes are not used.
GPIO [7:0]	-	I/O	4 mA	General purpose I/O Pins. These pins are GPIOs in all modes. GPIO5 is used as ISA-16-68_Mode select pin.
STROBEn	PP	O	11 mA	Set active low by the host to transfer data into the input latch of the peripheral. Data is valid while STROBEn is low
AUTOLFn	PP	O	11 mA	The interpretation of this signal varies from peripheral to peripheral. Set low by host to put some printers into auto-line feed mode

Table 7: Multiplexed Signals Description (Contd.)

Signal Name	Group	Type	Drive Strength	Description
INITn	PP	O	11 mA	Initialize the Peripheral / printer (open drain, active low). When set low, the peripheral or printer starts it's initialization routine
SELECTINn	PP	O	11 mA	Set low by host to select peripheral
ACKn	PP	I	4 mA	Pulsed low by the peripheral to acknowledge transfer of a data byte from the host
BUSY	PP	I	4 mA	Driven high by the peripheral to indicate that it is not ready to receive data
PAPEREND	PP	I	4 mA	Driven high by the peripheral to indicate that is has encountered an error in its paper path. The meaning of this signal varies from peripheral to peripheral. Peripherals shall set ERRORn/ FAULTn low whenever PAPEREND is set high
SELECT	PP	I	4 mA	Set high to indicate that the peripheral is online
ERRORn/ FAULTn	PP	I	4 mA	Set low by the peripheral to indicate that an error has occurred. The meaning of this signal varies from peripheral to peripheral
PPD [7:0]	PP	I/O	11 mA	Driven by the host in Compatibility Mode and the negotiation phase, not used in Nibble Mode, and bidirectional in all other modes
PP_DIR	PP	O	4 mA	Set low to indicate a data transfer direction of peripheral to host and set high to indicate a data transfer direction of host to peripheral
PERI_LOGIC_H	PP	I	4 mA	Set high to indicate that all other signals sourced by the peripheral are in a valid state. Set low to indicate that the peripheral power is off or that peripheral-driven interface signals are otherwise in an invalid state.
HOST_LOGIC_H	PP	O	4 mA	Set high to indicate that all other signals sourced by the host are in a valid state. Set low to indicate the host power is off or host-driven interface signals are otherwise in an invalid state
A [2:0]	ISA	O	11 mA	External Peripheral Address Lines

Table 7: Multiplexed Signals Description (Contd.)

Signal Name	Group	Type	Drive Strength	Description
IORn	ISA	O	11 mA	Active-low external peripheral I/O read signal
IOWn	ISA	O	4 mA	Active-low external peripheral I/O write signal
CSAn	ISA	O	4 mA	Chip select line to select one of the ports of external peripheral
CSBn	ISA	O	4 mA	Chip select line to select one of the ports of external peripheral
CSCn	ISA	O	4 mA	Chip select line to select one of the ports of external peripheral
CSDn	ISA	O	4 mA	Chip select line to select one of the ports of external peripheral
INTA	ISA	I	11 mA	Interrupt line for one of the ports of external peripheral
INTB	ISA	I	11 mA	Interrupt line for one of the ports of external peripheral
INTC	ISA	I	11 mA	Interrupt line for one of the ports of external peripheral
INTD	ISA	I	11 mA	Interrupt line for one of the ports of external peripheral
RESET	ISA	O	11 mA	External Peripheral Reset Signal.
A_10	ISA	O	11 mA	Extra address line used to configure ECP mode when external parallel peripheral requires extra address line to configure its ECP mode ports.
ISAD [1:0]	ISA	I/O	11 mA	External Peripheral Data Bus
ISAD [7:2]	ISA	I/O	4 mA	External Peripheral Data Bus
MODE_16_68N	ISA	O	4 mA	Mode select signal for external peripherals. When it is high 16-Mode (Intel) data bus interface is selected. When it is low 68-Mode (Motorola) data bus interface is selected. This is GPIO5 Pin.

Table 7: Multiplexed Signals Description (Contd.)

Signal Name	Group	Type	Drive strength	Description
PHY_CLOCK	USB	I	4 mA	USB PHY clock. 60Mhz Interface clock generated from External PHY. All the interface signals are synchronized with this clock.
USBD [7:0]	USB	I/O	4 mA	Bi-directional data bus, driven all zero's by the USB host link when it is idle. Bus ownership determined by DIR signal
DIR	USB	I	4 mA	Direction, controls transfer on data. 0: USB host link will transfer data to PHY. 1: PHY will transfer data to link
STP	USB	O	4 mA	Link asserts this signal for one clock cycle to stop data stream currently on the bus.
NXT	USB	I	4 mA	PHY asserts this to throttle the data
PHY_RESET	USB	O	4 mA	USB – PHY reset
PORT_ POWER_EN	USB	O	4 mA	External Power enable signal to the ULPI PHY 1 : Power enabled 0 : Power disabled
FAULT_LEVEL	USB	I	4 mA	Indicates fault level by the PHY
Not Used	-	-	-	No function defined in that mode
NC	-	-	-	No connection.

14. Architectural Overview

14.1 Brief Description Of Block Diagram

MCS9901 consists of 3 major blocks, namely: PCI Express End-point Controller, Bridge (MSIF and TSIF) and Device core. The device core consists of the following major blocks and Peripherals:

- TXDMA block
- RXDMA block
- 4 Serial ports
- Parallel port
- ISA
- USB Host Controller

14.2 PCI Express End Point Controller

PCI Express Endpoint is a device similar to PCI/PCI-X based Host Bus adapters. The Root port establishes the link up, initiates credits and then enumerates the Endpoint before Endpoint starts any memory write/read cycles. This PCI Express End-point is fully compliant with PCI Express base 1.0a specifications.

PCI Express architecture is classified into three layers namely transaction layer, data link layer, and physical layer. PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The software layers will generate Read and Write requests that are transported by the transaction layer to the I/O devices using a packet-based, Split Transaction Protocol. The link layer adds sequence numbers and CRC to these packets to create a highly reliable data transfer mechanism. The basic physical layer consists of a dual-simplex channel that is implemented as a Transmit pair and a Receive pair. The initial speed of 2.5 Gbps/direction provides a 200MBps communications channel that is close to twice that of classic PCI data rate.

Key Features of PCIe End-Point Controller

- VC0 is always supported.
- Boosts performance by launching multiple DMA read transactions
- Supports Four functions in a single device
- Auto Completion of configuration requests
- Built-in flow control
- Message TLP (Error) generation
- Integrated time-out handling of Non-posted requests
- Both legacy and MSI Interrupt supported

14.3 Bridge

The main function of the bridge is to maintain a link between PCIe and device core including all the peripherals configured on the other side of PCIe. The Bridge also takes care of all the interrupt logics i.e., generation, acknowledgments etc. It mainly includes two blocks to form a channel between PCIe and the device core i.e., Master Interface (MSIF) & Application Slave Interface (TSIF).

Master slave Interface (MSIF) is the block between the device core and PCIe Core. It converts all the device core transactions to make them PCIe compatible. It forms the header for the DMA transactions. It generates the interrupts on INTA, INTB, INTC, and INTD. It also generates interrupts through MSI (Message Signal Interrupt) mechanism.

Target Slave Interface (TSIF) is used to configure the registers of the peripherals.

14.4 Device Core

Device core contains all the peripherals i.e. four serial ports, one parallel port, ISA interface, USB Host Controller (OHCI and EHCI) and TXDMA & RXDMA.

14.4.1 TXDMA Block

This block transfers data from system memory to peripherals.

14.4.2 RXDMA Block

This block transfers data from peripherals to system memory.

14.4.3 Serial Port

The Serial port implemented in the MCS9901 is compatible with 16C 450/550/Ex 550 UART modes. Serial port controllers can be interfaced to external RS232/RS422/RS485 transceivers. Serial Port module consists of TXDMA, RXDMA and UART core. The TXDMA requests the data from system memory through DMA. This data which is coming from system memory, goes into TX FIFO. 8 bit data from the TX FIFO controllers goes to the UART core, which will convert this 8-bit data to serial data.

Similarly RXDMA enables data transfer from the peripheral to system memory. Data coming from the peripheral goes into RX FIFO and then into system memory. 256 bytes of TX FIFO & 256 bytes of RX FIFO are used in MCS9901 for each Serial Port. These deeper FIFOs enable faster device operation and less CPU Load.

14.4.4 Parallel Port

The parallel port of MCS9901 implements the IEEE 1284 compliant standard parallel port. Accordingly, all of the following various IEEE1284 modes below are supported:

- Nibble Mode
- Byte Mode
- Enhanced Parallel Port (EPP 1.9)
- Extended Capability Port (ECP) with and without RLE
- FIFO mode(Buffered SPP modes)

14.4.5 ISA Interface

An ISA bridge allows the product designer to increase the number of I/O ports through the use of external components. Here, additional UARTs and Parallel Ports are easy to attach and configure. The ISA bus operates at 8MHz with an 8-bit data bus. ISA interface supports both Intel and Motorola mode of data bus.

Following I/O expansion is feasible through MCS9901 ISA Interface:

- 1 Serial Port
- 2 Serial Ports
- 3 Serial ports
- 4 Serial ports
- 1 Serial + 1 Parallel Port
- 2 Serial + 1 Parallel Port

14.4.6 USB Host controller

USB 2.0 Host Controller includes one high-speed mode host controller and one USB 1.1 host controller. The high-speed host controller implements an EHCI interface which provides connectivity for all high-speed devices. A Companion Host Controller (OHCI) is used to manage full- and low- speed USB devices.

USB 2.0 host controller features are the following:

- USB 2.0/EHCI and OHCI Specification compliant
- Supports high-speed (480 Mbps), full-speed (12 Mbps) & low-speed (1.5Mbps) devices
- Supports ULPI PHY interface
- Supports up to 127 devices
- Supports Control, Bulk and Isochronous and interrupt data transfer types

15. Configuration Registers

The following are the configuration register values that are loaded into PCI Express configuration space when EEPROM is not present.

15.1 Function 0

Register Name	Offset	Default		Description
Dev Ven ID	0x000	**Opmode**	**Value**	This register contains Device and Vendor ID information.
		4SP	0x9901_9710	
		2SP_1PP	0x9901_9710	
		2SP_ISA	0x9901_9710	
		USB_2SP	0x9902_9710	
		USB_2PP	0x9902_9710	
		USB_1PP	0x9902_9710	
		USB	0x9920_9710	
Class code. REV ID	0x004	**Opmode**	**Value**	This register contains Class code and Revision ID information.
		4SP	0x0700_0200	
		2SP_1PP	0x0700_0200	
		2SP_ISA	0x0700_0200	
		USB_2SP	0x0C03_1000	
		USB_1PP	0x0C03_1000	
		USB_ISA	0x0C03_1000	
		USB	0x0C03_1000	

Register Name	Offset	Default		Description
Bar 0	0x008	**Opmode**	**Value**	BAR0 value
		4SP	0xFFFF_FFF9	
		2SP_1PP	0xFFFF_FFF9	
		2SP_ISA	0xFFFF_FFF9	
		USB_2SP	0xFFFF_F000	
		USB_1PP	0xFFFF_F000	
		USB_ISA	0xFFFF_F000	
		USB	0xFFFF_F000	
Bar1	0x00C	**Opmode**	**Value**	BAR1 value
		4SP	0x0000_0000	
		2SP_1PP	0x0000_0000	
		2SP_ISA	0x0000_0000	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	
Bar2	0x010	**Opmode**	**Value**	BAR2 value
		4SP	0x0000_0000	
		2SP_1PP	0x0000_0000	
		2SP_ISA	0x0000_0000	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	

Register Name	Offset	Default		Description
Bar3	0x014	**Opmode**	**Value**	BAR3 value
		4SP	0x0000_0000	
		2SP_1PP	0x0000_0000	
		2SP_ISA	0x0000_0000	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	
Bar4	0x018	**Opmode**	**Value**	BAR4 value
		4SP	0xFFFF_F000	
		2SP_1PP	0xFFFF_F000	
		2SP_ISA	0xFFFF_F000	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	
Sub Sys ID- Sub Sys Ven ID	0x01C	**Opmode**	**Value**	Contains information about sub system device ID vendor ID.
		4SP	0x1000_A000	
		2SP_1PP	0x1000_A000	
		2SP_ISA	0x1000_A000	
		USB_2SP	0x4000_A000	
		USB_2PP	0x4000_A000	
		USB_1PP	0x4000_A000	
		USB	0x4000_A000	
INTR. Pin Matching	0x020	0x0000_0100		Interrupt pin mapping information.
Power mgmt. Cpbl. Register.	0x024	0xFFC3_D001		Contains information Power Mgmt. Capabilities

Register Name	Offset	Default		Description
Device Cpbl. Register.	0x028	**Opmode**	**Value**	Contains information about device capabilities.
		4SP	0x0000_8001	
		2SP_1PP	0x0000_8001	
		2SP_ISA	0x0000_8001	
		USB_2SP	0x0000_8003	
		USB_1PP	0x0000_8003	
		USB_ISA	0x0000_8003	
		USB	0x0000_8003	
Link. Cpbl. Reg.	0x02C	0x0003_FC11	Link information.	Link. Cpbl. Reg.

15.2 Function 1

Register Name	Offset	Default		Description
Dev Ven ID	0x030	**Opmode**	**Value**	This register contains Device and Vendor ID information.
		4SP	0x9901_9710	
		2SP_1PP	0x9901_9710	
		2SP_ISA	0x9901_9710	
		USB_2SP	0x9902_9710	
		USB_2PP	0x9902_9710	
		USB_1PP	0x9902_9710	
		USB	0x9920_9710	

Register Name	Offset	Default		Description
Class code. Rev ID	0x034	**Opmode**	**Value**	This register contains Class code and Revision ID information.
		4SP	0x0700_0200	
		2SP_1PP	0x0700_0200	
		2SP_ISA	0x0700_0200	
		USB_2SP	0x0C30_2000	
		USB_1PP	0x0C30_2000	
		USB_ISA	0x0C30_2000	
		USB	0x0C30_2000	
Bar 0	0x038	**Opmode**	**Value**	BAR0 Value.
		4SP	0xFFFF_FFF9	
		2SP_1PP	0xFFFF_FFF9	
		2SP_ISA	0xFFFF_FFF9	
		USB_2SP	0xFFFF_FF00	
		USB_1PP	0xFFFF_FF00	
		USB_ISA	0xFFFF_FF00	
		USB	0xFFFF_FF00	
Bar1	0x03C	**Opmode**	**Value**	BAR1 value.
		4SP	0xFFFF_F000	
		2SP_1PP	0xFFFF_F000	
		2SP_ISA	0xFFFF_F000	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	

Register Name	Offset	Default		Description
Bar2	0x040	**Opmode**	**Value**	BAR2 value.
		4SP	0x0000_0000	
		2SP_1PP	0x0000_0000	
		2SP_ISA	0x0000_0000	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	
Bar3	0x044	**Opmode**	**Value**	BAR3 value.
		4SP	0x0000_0000	
		2SP_1PP	0x0000_0000	
		2SP_ISA	0x0000_0000	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	
Bar4	0x048	**Opmode**	**Value**	BAR4 value.
		4SP	0xFFFF_F000	
		2SP_1PP	0xFFFF_F000	
		2SP_ISA	0xFFFF_F000	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	

Register Name	Offset	Default		Description
Sub Sys ID- Sub Sys Ven ID	0x04C	**Opmode**	**Value**	Contains information about sub system device ID vendor ID.
		4SP	0x1000_A000	
		2SP_1PP	0x1000_A000	
		2SP_ISA	0x1000_A000	
		USB_2SP	0x4000_A000	
		USB_2PP	0x4000_A000	
		USB_1PP	0x4000_A000	
		USB	0x4000_A000	
		4SP	0x1000_A000	
INTR. Pin Matching	0x050	0x0000_0200		Interrupt pin mapping information.
Power mgmt. Cpbl. Register.	0x054	0xFFC3_D001		Contains information on Power Mgmt. Capabilities
Device Cpbl. Register.	0x058	**Opmode**	**Value**	Contains information about device capabilities.
		4SP	0x0000_8001	
		2SP_1PP	0x0000_8001	
		2SP_ISA	0x0000_8001	
		USB_2SP	0x0000_8003	
		USB_1PP	0x0000_8003	
		USB_ISA	0x0000_8003	
		USB	0x0000_8003	
Link. Cpbl. Reg.	0x05C	0x0003_FC11		Link information.

15.3 Function 2

Register Name	Offset	Default		Description
Dev Ven ID	0x060	**Opmode**	**Value**	This register contains Device and Vendor ID information.
		4SP	0x9901_9710	
		2SP_1PP	0x9901_9710	
		2SP_ISA	0xFFFF_FFFF	
		USB_2SP	0x9902_9710	
		USB_1PP	0x9902_9710	
		USB_ISA	0xFFFF_FFFF	
		USB	0xFFFF_FFFF	
Class code. Rev ID	0x064	**Opmode**	**Value**	This register contains Class code and Revision ID information.
		4SP	0x0700_0200	
		2SP_1PP	0x0701_0300	
		2SP_ISA	0x0000_0000	
		USB_2SP	0x0700_0200	
		USB_1PP	0x0701_0300	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	
Bar 0	0x068	**Opmode**	**Value**	BAR0 Value.
		4SP	0xFFFF_FFF9	
		2SP_1PP	0xFFFF_FFF9	
		2SP_ISA	0x0000_0000	
		USB_2SP	0xFFFF_FFF9	
		USB_1PP	0xFFFF_FFF9	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	

Register Name	Offset	Default		Description
Bar1	0x06C	**Opmode**	**Value**	BAR1 Value
		4SP	0xFFFF_F000	
		2SP_1PP	0xFFFF_FFFD	
		2SP_ISA	0x0000_0000	
		USB_2SP	0xFFFF_F000	
		USB_1PP	0xFFFF_FFFD	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	
Bar2	0x070	**Opmode**	**Value**	BAR2 Value
		4SP	0xFFFF_F004	
		2SP_1PP	0xFFFF_F004	
		2SP_ISA	0x0000_0000	
		USB_2SP	0xFFFF_F004	
		USB_1PP	0xFFFF_F004	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	
Bar3	0x074	**Opmode**	**Value**	BAR3 Value
		4SP	0xFFFF_FFFF	
		2SP_1PP	0xFFFF_FFFF	
		2SP_ISA	0x0000_0000	
		USB_2PP	0xFFFF_FFFF	
		USB_1PP	0xFFFF_FFFF	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	

Register Name	Offset	Default		Description
Bar4	0x078	**Opmode**	**Value**	BAR4 Value
		4SP	0x0000_0000	
		2SP_1PP	0xFFFF_F000	
		2SP_ISA	0x0000_0000	
		USB_2SP	0x0000_0000	
		USB_1PP	0xFFFF_F000	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	
Sub Sys ID- Sub Sys Ven ID	0x07C	**Opmode**	**Value**	Contains information about sub system device ID vendor ID.
		4SP	0x1000_A000	
		2SP_1PP	0x2000_A000	
		2SP_ISA	0x1000_A000	
		USB_2SP	0x4000_A000	
		USB_1PP	0x4000_A000	
		USB_ISA	0x4000_A000	
		USB	0x4000_A000	
INTR. Pin Matching	0x080	0x0000_0300		Interrupt pin mapping information.
Power mgmt. Cpbl. Register.	0x084	0xFFC3_D001		Contains information on Power Mgmt. Capabilities
Device Cpbl. Register.	0x088	**Opmode**	**Value**	Contains information about device capabilities.
		4SP	0x0000_8001	
		2SP_1PP	0x0000_8001	
		2SP_ISA	0x0000_8001	
		USB_2SP	0x0000_8001	
		USP_1PP	0x0000_8001	
		USB_ISA	0x0000_8001	
		USB	0x0000_8001	

Register Name	Offset	Default	Description
Link. Cpbl. Reg.	0x08C	0x0003_FC11	Link information.

15.4 Function 3

Register Name	Offset	Default		Description
Dev Ven ID	0x090	**Opmode**	**Value**	This register contains Device and Vendor ID information.
		4SP	0x9901_9710	
		2SP_1PP	0xFFFF_FFFF	
		2SP_ISA	0x9901_9710	
		USB_2SP	0x9902_9710	
		USB_1PP	0xFFFF_FFFF	
		USB_ISA	0x9902_9710	
		USB	0xFFFF_FFFF	
Class code. Rev ID	0x094	**Opmode**	**Value**	This register contains Class code and Revision ID information.
		4SP	0x0700_0200	
		2SP_1PP	0x0000_0000	
		2SP_ISA	0x0780_0000	
		USB_2SP	0x0700_0600	
		USB_1PP	0x0000_0000	
		USB_ISA	0x0780_0000	
		USB	0x0000_0000	

Register Name	Offset	Default		Description
Bar 0	0x098	**Opmode**	**Value**	BAR0 Value
		4SP	0xFFFF_FFF9	
		2SP_1PP	0x0000_0000	
		2SP_ISA	0xFFFF_FFF9	
		USB_2SP	0xFFFF_FFF9	
		USB_1PP	0x0000_0000	
		USB_ISA	0xFFFF_FFF9	
		USB	0x0000_0000	
Bar1	0x09C	**Opmode**	**Value**	BAR1 Value
		4SP	0xFFFF_F000	
		2SP_1PP	0x0000_0000	
		2SP_ISA	0xFFFF_FFF9	
		USB_2SP	0xFFFF_F000	
		USB_1PP	0x0000_0000	
		USB_ISA	0xFFFF_FFF9	
		USB	0x0000_0000	
Bar2	0x0A0	**Opmode**	**Value**	BAR2 Value
		4SP	0x0000_0000	
		2SP_1PP	0x0000_0000	
		2SP_ISA	0xFFFF_FFF9	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0xFFFF_FFF9	
		USB	0x0000_0000	

Register Name	Offset	Default		Description
Bar3	0x0A4	**Opmode**	**Value**	BAR3 Value
		4SP	0x0000_0000	
		2SP_1PP	0x0000_0000	
		2SP_ISA	0xFFFF_FFF9	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0xFFFF_FFF9	
		USB	0x0000_0000	
Bar4	0x0A8	**Opmode**	**Value**	BAR4 Value
		4SP	0xFFFF_F000	
		2SP_1PP	0xFFFF_F000	
		2SP_ISA	0xFFFF_F000	
		USB_2SP	0x0000_0000	
		USB_1PP	0x0000_0000	
		USB_ISA	0x0000_0000	
		USB	0x0000_0000	
Sub Sys ID- Sub Sys Ven ID	0x0AC	**Opmode**	**Value**	Contains information about sub system device ID vendor ID.
		4SP	0x1000_A000	
		2SP_1PP	0xFFFF_FFFF	
		2SP_ISA	0x3004_A000	
		USB_2SP	0x1000_A000	
		USB_1PP	0xFFFF_FFFF	
		USB_ISA	0x3004_A000	
		USB	0xFFFF_FFFF	
INTR. Pin Matching	0x0B0	0x0000_0400		Interrupt pin mapping information.
Power mgmt. Cpbl. Register.	0x0B4	0xFFC3_D001		Contains information Power Mgmt. Capabilities

Register Name	Offset	Default		Description
Device Cpbl. Register.	0x0B8	**Opmode**	**Value**	Contains information about device capabilities.
		4SP	0x0000_8001	
		2SP_1PP	0x0000_8001	
		2SP_ISA	0x0000_8001	
		USB_2SP	0x0000_8001	
		USB_1PP	0x0000_8001	
		USB_ISA	0x0000_8001	
		USB	0x0000_8001	
Link. Cpbl. Reg.	0x0BC	0x0003_FC11		Link information.

16. EEPROM Content Layout

Bytes	# of Bytes	Name	Value for PCIe to 4 Serial (Hex)	Description
[1:0]	2	Signature	97-10	Detects Presence of EEPROM.For loading configuration through EEPROM, Signature content should be "0x9710" else default configuration will be loaded from MCS9901.
Function-0				
[3:2]	2	Vendor ID0	97-10	This field identifies the Manufacturer of the Device. Change of this value requires software drive modification.
[5:4]	2	Device ID0	99-01	This field identifies the particular device allocated by the vendor. Section 15 shows the valid options. Change of this value requires software drive modification.
6	1	Rev. ID0	00	Device Specific Revision identifier.
7	3	Register level programming interface0	02	Class Code -16C550 Compatible serial controller. Simple Communication Controller.
8		Sub-Class code0	00	
9		Base Class Code0	07	
[13:10]	4	Bar-0 of Function-0	FF-FF-FF-F9	Function-0 Bar Registers. Refer to Section 15 for other Modes.
[17:14]	4	Bar-1 of Function-0	FF-FF-F0-00	
[21:18]	4	Bar-2 of Function-0	00-00-00-00	
[25:22]	4	Bar-3 of Function-0	00-00-00-00	
[29:26]	4	Bar-4 of Function-0	FF-FF-F0-00	
[31:30]	2	Sub-System Vendor ID0	A0-00	This register is used to identify the subsystem where the PCIe device resides. Refer to Section 15 for Sub-System ID.
[33:32]	2	Sub-System ID0	10-00	

Bytes	# of Bytes	Name	Value for PCIe to 4 Serial (Hex)	Description
34	1	Interrupt Line0	00	It is used to communicate interrupt line routing information. The value in this register tells which input of the system interrupt controller the device's interrupt pin is connected to. Don't change this value.
35	1	Interrupt Pin0	01	The interrupt pin register tells which interrupt PIN the device uses. A value of 0x01 corresponds to **INTA#**.
36	1	Min_Gnt0	00	Not applicable to PCIe. Don't change this value.
37	1	Max_Lat0	00	Not applicable to PCIe. Don't change this value.
[41:38]	4	Power Management0	FF-C3-D0-01	Power Management Capability Information. Don't change this value.
[45:42]	4	Device Capability0	00-00-80-01	For identification of PCIe device function and to provide access to PCIe Specific control/status registers and related power management enhancements. Refer to Section 15.
[49:46]	4	Link Capability0	00-03-FC-11	Link Capability registers providing access to Status/ control of Links. Don't change this value.
Function-1				
[51:50]	2	Vendor ID1	97-10	This field identifies the Manufacturer of the Device. Change in this value requires software drive modification.
[53:52]	2	Device ID1	99-01	This field identifies the particular Device, allocated by the vendor. Section 15 shows the valid options. Change of this value requires software drive modification.
54	1	Rev. ID1	00	Device Specific Revision identifier.

Bytes	# of Bytes	Name	Value for PCIe to 4 Serial (Hex)	Description
55	3	Register level programming interface1	02	Class Code - 16C550 Compatible serial controller. Simple Communication Controller.
56		Sub-Class code1	00	
57		Base Class Code1	07	
[61:58]	4	Bar-0 of Function-1	FF-FF-FF-F9	Function-1 Bar Registers. Refer to Section 15 for other Modes.
[65:62]	4	Bar-1 of Function-1	FF-FF-F0-00	
[69:66]	4	Bar-2 of Function-1	00-00-00-00	
[73:70]	4	Bar-3 of Function-1	00-00-00-00	
[77:74]	4	Bar-4 of Function-1	FF-FF-F0-00	
[79:78]	2	Sub-System Vendor ID1	A0-00	This register is used to identify the subsystem where the PCIe device resides. Refer to Section 15 for Sub-System ID.
[81:80]	2	Sub-System Device ID1	10-00	
82	1	Interrupt Line1	00	It is used to communicate interrupt line routing information. The value in this register tells which input of the system interrupt controller the device's interrupt pin is connected to. Don't change this value.
83	1	Interrupt Pin1	02	The interrupt pin register tells which interrupt PIN the device uses. A value of 0x02 corresponds to **INTB#**.
84	1	Min_Gnt1	00	Not applicable to PCIe. Don't change this value.
85	1	Max_Lat1	00	Not applicable to PCIe. Don't change this value.
[89:86]	4	Power Management1	FF-C3-D0-01	Power Management Capability Information. Don't change this value.

Bytes	# of Bytes	Name	Value for PCIe to 4 Serial (Hex)	Description
[93:90]	4	Device Capability1	00-00-80-01	For identification of PCIe device function and to provide access to PCIe Specific control/status registers and related power management enhancements. Refer to Section 15.
[97:94]	4	Link Capability1	00-03-FC-11	Link Capability registers providing access to Status/ control of Links. Don't change this value.
Function-2				
[99:98]	2	Vendor ID2	97-10	This field identifies the Manufacturer of the Device. Change in this value requires software drive modification.
[101:100]	2	Device ID2	99-01	This field identifies the particular Device, allocated by the vendor. Section 15 shows the valid options. Change of this value requires software drive modification.
102	1	Rev. ID2	00	Device Specific Revision identifier.
103	3	Register level programming interface2	02	Class Code - 16C550 Compatible serial controller. Simple Communication Controller.
104		Sub-Class code2	00	
105		Base Class Code2	07	
[109:106]	4	Bar-0 of Function-2	FF-FF-FF-F9	Function-2 Bar Registers. Refer to Section 15 for other Modes.
[113:110]	4	Bar-1 of Function-2	FF-FF-F0-00	
[117:114]	4	Bar-2 of Function-2	00-00-00-00	
[121:118]	4	Bar-3 of Function-2	00-00-00-00	
[125:122]	4	Bar-4 of Function-2	FF-FF-F0-00	

Bytes	# of Bytes	Name	Value for PCIe to 4 Serial (Hex)	Description
[127:126]	2	Sub-System Vendor ID2	A0-00	This register is used to identify the subsystem where the PCIe device resides. Refer to Section 15 for Sub-System ID.
[129:128]	2	Sub-System Device ID2	10-00	
130	1	Interrupt Line2	00	It is used to communicate interrupt line routing information. The value in this register tells which input of the system interrupt controller the device's interrupt pin is connected to. Don't change this value.
131	1	Interrupt Pin2	03	The interrupt pin register tells which interrupt PIN the device uses. A value of 0x03 corresponds to **INTC#**.
132	1	Min_Gnt2	00	Not applicable to PCIe. Don't change this value.
133	1	Max_Lat2	00	Not applicable to PCIe. Don't change this value.
[137:134]	4	Power Management2	FF-C3-D0-01	Power Management Capability Information. Don't change this value.
[141:138]	4	Device Capability2	00-00-80-01	For identification of PCIe device function and to provide access to PCIe Specific control/status registers and related power management enhancements. Refer to Section 15.
[145:142]	4	Link Capability2	00-03-FC-11	Link Capability registers providing access to Status/ control of Links. Don't change this value.
Function-3				
[147:146]	2	Vendor ID3	97-10	This field identifies the Manufacturer of the Device. Change in this value requires software drive modification.

Bytes	# of Bytes	Name	Value for PCIe to 4 Serial (Hex)	Description
[149:148]	2	Device ID3	99-01	This field identifies the particular Device, allocated by the vendor. Section 15 shows the valid options. Change of this value other than this table requires software drive modification.
150	1	Rev. ID3	00	Device Specific Revision identifier.
151	3	Register level programming interface3	02	Class Code - 16C550 Compatible serial controller. Simple Communication Controller.
152		Sub-Class code3	00	
153		Base Class Code3	07	
[157:154]	4	Bar-0 of Function-3	FF-FF-FF-F9	Function-3 Bar Registers. Refer to Section 15 for other Modes.
[161:158]	4	Bar-1 of Function-3	FF-FF-F0-00	
[165:162]	4	Bar-2 of Function-3	00-00-00-00	
[169:166]	4	Bar-3 of Function-3	00-00-00-00	
[173:170]	4	Bar-4 of Function-3	FF-FF-F0-00	
[175:174]	2	Sub-System Vendor ID3	A0-00	This register is used to identify the subsystem where the PCIe device resides. Refer to Section 15 for Sub-System ID.
[177:176]	2	Sub-System Device ID3	10-00	
178	1	Interrupt Line3	00	It is used to communicate interrupt line routing information. The value in this register tells which input of the system interrupt controller the device's interrupt pin is connected to. Don't change this value.
179	1	Interrupt Pin3	04	The interrupt pin register tells which interrupt PIN the device uses. A value of 0x04 corresponds to **INTD#**.

Bytes	# of Bytes	Name	Value for PCIe to 4 Serial (Hex)	Description
180	1	Min_Gnt3	00	Not applicable to PCIe. Don't change this value.
181	1	Max_Lat3	00	Not applicable to PCIe. Don't change this value.
[185:182]	4	Power Management3	FF-C3-D0-01	Power Management Capability Information. Don't change this value.
[189:186]	4	Device Capability3	00-00-80-01	For identification of PCIe device function and to provide access to PCIe Specific control/status registers and related power management enhancements. Refer to Section 15.
[193:190]	4	Link Capability3	00-03-FC-11	Link Capability registers providing access to Status/ control of device Links. Don't change this value.
Serial Number for PCIe				
[201:194]	8	Serial Number	88-99-FF-EE- DD-CC-BB-AA	Device Serial number. Don't change this value.
USB Register SET (Don't change this values.)				
[205:202]	4	OC Sample Count	00-09-27-C0	OC Sample Count : This count value is kept for Detection of over current Condition
[209:206]	4	Host Disconnect Count	00-03-0D-40	Host Disconnect Count : This count value Counts the host disconnect Time
[213:210]	4	Restart Timeout count	00-00-CF-08	Restart Timeout count : Count value to re-entering suspend state when proper resume event is not detected
[217:214]	4	TD Disconnect Count	00-00-00-96	TD Disconnect Count : Time to detect a disconnect event at a hub's downstream facing port
[221:218]	4	TD Reset Count	00-09-20-00	TD Reset Count : This is the period of time hubs drive reset to a device
[225:222]	4	TUCHEND Count	00-06-68-4C	TUCHEND Count : Time after start of SE0 by which a high-Speed capable device is required to have completed its Chirp K within the reset protocol

Bytes	# of Bytes	Name	Value for PCIe to 4 Serial (Hex)	Description
[229:226]	4	TFILT Count	00-00-00-A0	TFILT Count : Time for which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake
[233:230]	4	TDCHBIT Count	00-00-0C-00	TDCHBIT Count : Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset
[237:234]	4	TDCHSE0 Count	00-00-27-10	TDCHSE0 Count : Time before end of reset by which a hub must end its downstream chirp sequence
[241:238]	4	TWTDCH Count	00-00-17-70	TWTDCH Count : Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence
[245:242]	4	LS_WAIT Count	00-00-02-80	LS_WAIT Count : Time value to exit from Resume state for LS device
[249:246	4	PIE_TX_ TOKEN Count_0	00-00-00-03	PIE_TX_TOKEN Count_0 : IPG time for Hs/Fs token broadcast
[253:250]	4	OHCI_0_ TIMEOUT_ PERIOD	00-00-00-FF	OHCI_0_TIMEOUT_PERIOD Count : Timeout value for FS IN data reception
[257:254]	4	OHCI_0_ TIMEOUT_ PERIOD_4_IN	00-00-00-FF	OHCI_0_TIMEOUT_PERIOD_4_IN Count : Timeout value for FS hsk reception
[261:258]	4	OHCI_0_LS_ TIMEOUT_ PERIOD	00-00-0F-FF	OHCI_0_LS_TIMEOUT_PERIOD Count: Timeout value for LS IN data reception
[265:262]	4	OHCI_0_LS_ TIMEOUT_ PERIOD_4_IN	00-00-0F-FF	OHCI_0_LS_TIMEOUT_PERIOD_4_IN Count : Timeout value for LS hsk reception
[269:266]	4	EHCI_PE_SM TOKEN	00-00-00-10	EHCI_PE_SM TOKEN Count : IPG time value for HS Token transmission
[273:270]	4	EHCI_PE_ SM DATAOUT Count	00-00-00-12	EHCI_PE_SM DATAOUT Count : IPG time value for HS DATA OUT transmission

Bytes	# of Bytes	Name	Value for PCIe to 4 Serial (Hex)	Description
[277:274]	4	PIE_TX_ TOKEN Count_1	00-00-00-50	PIE_TX_TOKEN Count_1 : IPG time for Ls token broadcast
[281:278]	4	TRANSACTION_ REQ	00-00-00-64	TRANSACTION_REQ Count : Transaction req timer value
[285:282]	4	UF Count	00-00-1D-2B	UF Count : MIFCRo frame count value
[289:286]	4	EHCI_ PIE TX_CNT	00-00-00-03	EHCI_PIE TX_CNT Count_0 : IPG value of HS token broadcast
[293:290]	4	EHCI_ TIMEOUT PERIOD	00-00-00-FF	EHCI_TIMEOUT PERIOD Count : Timeout value for HS IN data reception
[297:294]	4	EHCI_ TIMEOUT PERIOD_4_IN	00-00-00-FF	EHCI_TIMEOUT PERIOD_4_IN Count : Timeout value for HS HSK reception.
[301:298]	4	OHCI_ RESUME	00-16-E2-34	OHCI_RESUME Count : Resume time value.
[305:302]	4	HOST CONNECT	00-03-0D-40	HOST CONNECT Count : Host disconnect sampling time value for connect detection.
[309:306]	4	PIE_TX_HSK_ COUNT_0	00-00-00-03	PIE_TX_HSK_COUNT_0
[313:310]	4	PIE_TX_HSK_ COUNT_1	00-00-00-50	PIE_TX_HSK_COUNT_1
ISA Bridge Configuration and Interrupt Mask registers				
[315:314]	2	ISA Bridge Register	44-03	ISA Bridge Register.
316	1	PM Register	85	Power Management Register.
317	1	INTA-Mask	01	INTA Mask Register.
318	1	INTB-Mask	02	INTB Mask Register.
319	1	INTC-Mask	04	INTC Mask Register.
320	1	INTD-Mask	08	INTD Mask Register.

Note: BAR - Base Address Register.

17. Extended Modes through EEPROM

As explained in the earlier sections, MCS9901 can support 7 Peripheral configurations through mode select pins without using external EEPROM. These 7 Peripheral configurations are tabulated below.

S.No	Possible product Configuration	Is EEPROM Must?	Is Mode selection at system level required?
1	PCIe to 4 Serial	No	Yes
2	PCIe to 2 Serial + 1 Parallel	No	Yes
3	PCIe to 6 Serial = PCIe to 2 Serial + ISA (4 Serial)	No	Yes
4	PCIe to USB + 2 Serial	No	Yes
5	PCIe to USB + 1 Parallel	No	Yes
6	PCIe to USB + 4 Serial = PCIe to USB + ISA (4 Serial)	No	Yes
7	PCIe to USB only	No	Yes

By using external EEPROM, more Peripheral configurations can be derived with MCS9901. A few such configurations are listed below :

S.No	Possible product Configuration	Is EEPROM Must?	Is Mode selection at system level required?
1	PCIe to 1 Serial	Yes	Yes
2	PCIe to 2 Serial	Yes	Yes
3	PCIe to 3 Serial	Yes	Yes
4	PCIe to 5 Serial = PCIe to 2 Serial + ISA (3 Serial)	Yes	Yes
5	PCIe to 1 Serial + 1 Parallel	Yes	Yes

S.No	Possible product Configuration	Is EEPROM Must?	Is Mode selection at system level required?
6	PCIe to 3 Serial + 1 Parallel = PCIe to 2 Serial + ISA (1 Serial + 1 Parallel)	Yes	Yes
7	PCIe to 4 Serial + 1 Parallel = PCIe to 2 Serial + ISA (2 Serial + 1 Parallel)	Yes	Yes
8	PCIe to USB + 1 Serial	Yes	Yes
9	PCIe to USB + 3 Serial = PCIe to USB + ISA (3 Serial)	Yes	Yes
10	PCIe to USB + 1 Serial + 1 Parallel = PCIe to USB + ISA (1 Serial + 1 Parallel)	Yes	Yes
11	PCIe to USB + 2 Serial + 1 Parallel = PCIe to USB + ISA (2 Serial + 1 Parallel)	Yes	Yes

Vendor ID and Product ID customizations can also be implemented in the MCS9901, through external EEPROM.

18. Electrical Specifications

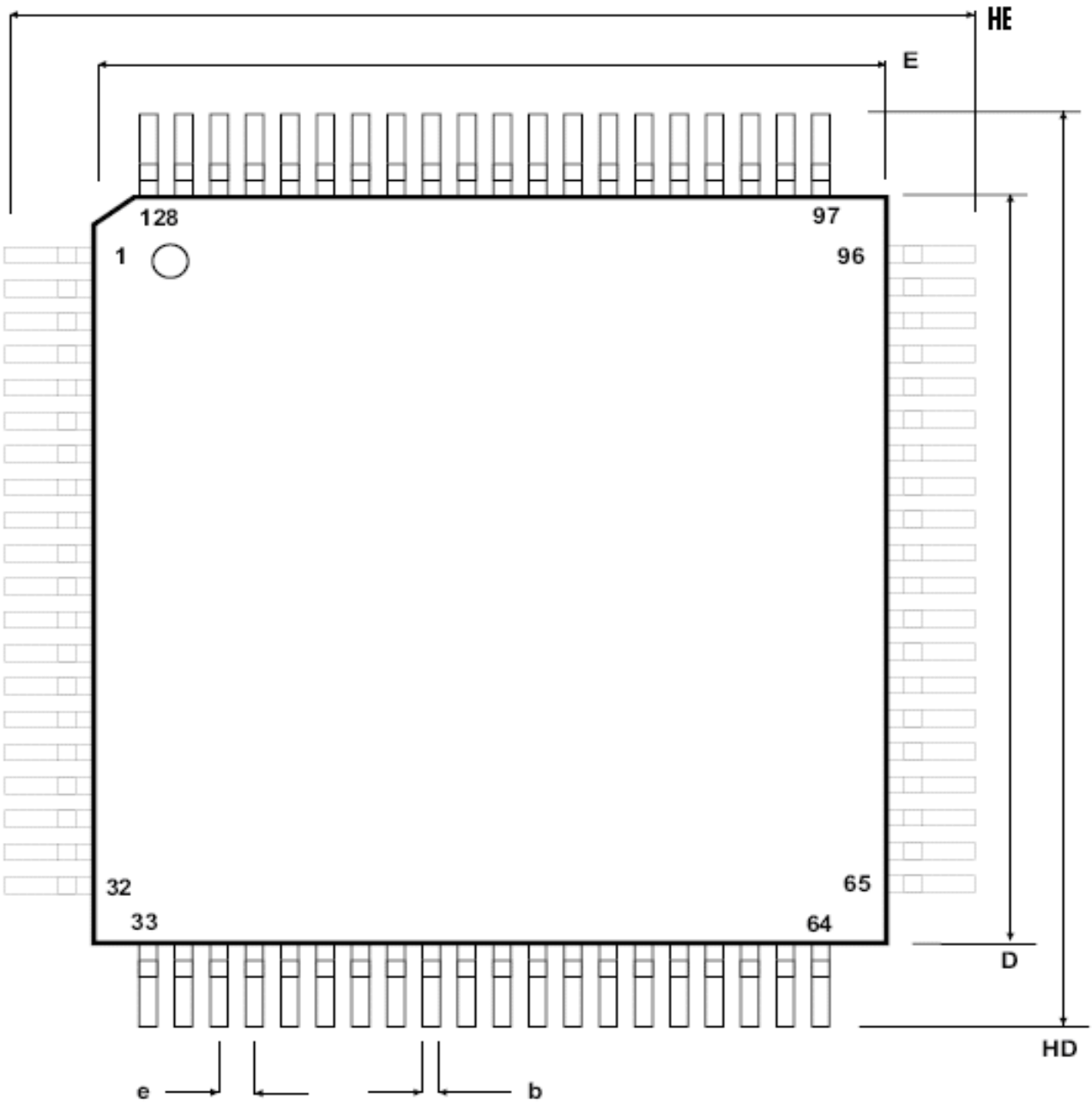
Absolute Maximum Ratings:

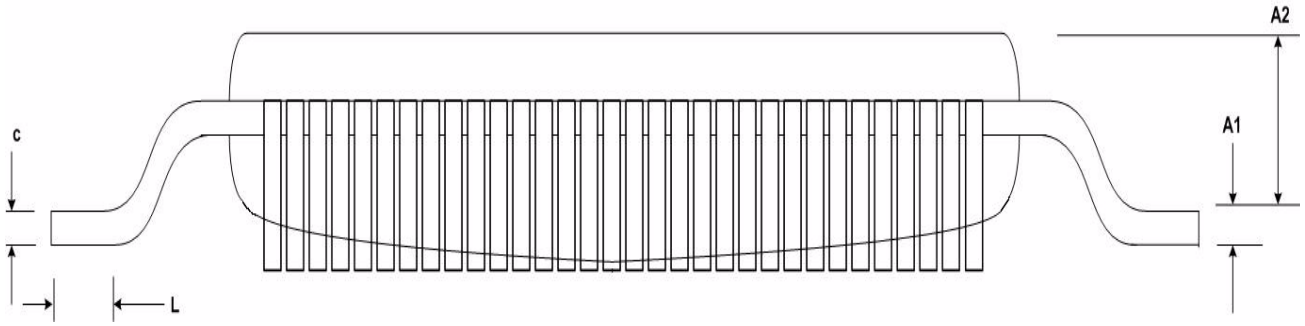
Symbols	Parameter	Rating	Units
VCC_K	Core Power Supply	-0.5 to 1.8	V
VccI0	Power Supply of 3.3V I/O	-0.5 to 3.63	V
T_O	Operating Temperature	0 to +70	°C
T_{STG}	Storage Temperature	-40 to +150 °C	°C
	ESD HBM (MIL-STD 883E Method 3015-7 Class 2)	2000	V
	ESD MM (JEDEC EIA/ JESD22A115-A)	200	V
	CDM (JEDEC/JESD22 C101-A)	500	V
VCC	Latch-up (JESD No. 78, March 1997) 200	1.4 X VCC	MA
T_j	Junction Temperature	115	°C

Operating Condition

Symbol	Parameter	Min	Typ	Max	Units
VCCIO	I/O Supply 3.3V - Digital	2.97	3.3	3.63	V
VCCA_3.3V	I/O Supply 3.3V - Analog	2.97	3.3	3.63	V
$VCCI^2C$	I^2C Supply – 1.2V	1.08	1.2	1.32	V
VCCK	Core Supply 1.2V - Digital	1.08	1.2	1.32	V
VCCA_1.2V	Core Supply 1.2V – Analog	1.08	1.2	1.32	V
VCCPLL	PLL Supply – 1.2V	1.08	1.2	1.32	V
Vin – I/O	Input Voltage of Peripheral I/O Pins – Serial, Parallel, ISA & USB interfaces	3.0	3.3	5	V
$I_{3.3v}$	Operating current of 3.3V (Analog and Digital)	-	30	-	mA
$I_{1.2v}$	Operating current of 1.2V (Analog and Digital)		150		mA

19. Mechanical Specification - QFP 128





128-Pin QFP
Package Dimensions

Symbol	Millimeters		
	MIN	TYP	MAX
A1	0.05		-
A2	1.35		1.45
b	0.13		0.23
c	0.09		0.20
e		0.40	
L	0.45		0.75
HD	15.85	16	16.15
D	13.90	14	14.10
HE	15.85	16	16.15
E	13.90	14	14.10

20. Contact Information

For Commercial information & availability write to : sales@moschip.com

For Technical information write to : techsupport@moschip.com

Revision History

Date	Reason for change	Version
18th Aug, 2007	Initial Release	0.6
24th Oct, 2007	Updated for addition of seven different pinout diagrams	0.7
02nd Nov, 2007	Datasheet updated for ASIC pinout changes	1.0
10th Jan 2008	Page 05 : Serial port Wake on ring feature removed Page 06 : Certifications data Modified. Page 57: Under Electrical Characteristics VCCI2C, Current Ratings modified.	1.1